What Is Claimed Is:

1. A method of forming an integrated circuit transistor, comprising:

proving a semiconductor substrate with a gate structure formed thereon;

forming at least one dielectric layer overlying the semiconductor substrate, wherein the at least one dielectric layer comprises at least one first portion along at least one sidewall of the gate structure, and at least one second portion outside the gate structure along the surface of the semiconductor substrate;

forming at least one first doped region in the semiconductor substrate laterally adjacent to the at least one first portion of the at least one dielectric layer, wherein the at least one second portion of the at least one dielectric layer remains overlying the at least one first doped region;

forming a sidewall spacer overlying the at least one dielectric layer along the at least one sidewall of the gate structure; and

forming at least one second doped region in the semiconductor substrate laterally adjacent to the sidewall spacer.

2. The method of forming an integrated circuit transistor of claim 1, wherein a thickness of the at least one dielectric layer ranges from about 10 Angstroms to about 350 Angstroms.

3. The method of forming an integrated circuit transistor of claim 1, further comprising a step of removing exposed regions of the at least one dielectric layer before the formation of the at least one second doped region.

4. The method of forming an integrated circuit transistor of claim 1, wherein the formation of the at least one dielectric layer is a blanket deposition of silicon oxide, silicon oxynitride, alternating layers of silicon oxide and silicon nitride, or combinations thereof.

5. The method of forming an integrated circuit transistor of claim 1, wherein the formation of the at least one dielectric layer is a blanket deposition by a chemical vapor deposition (CVD) process using tetraethylorthosilicate (TEOS).

6. The method of forming an integrated circuit transistor of claim 1, wherein the sidewall spacer is silicon oxide, silicon oxynitride, alternating layers of silicon oxide and silicon nitride, or combinations thereof.

7 The method of forming an integrated circuit transistor of claim 1, wherein the sidewall spacer is formed using a blanket deposition process and a dry etch process.

8. The method of forming an integrated circuit transistor of claim 1, wherein the at least one first doped region is formed using an ion implantation process and an annealing process.

9. The method of forming an integrated circuit transistor of claim 8, wherein after the annealing process, the at least one dielectric layer becomes a densified material which

exhibits an etch rate less than about 200 Angstroms/minute in a 100:1 HF solution.

10. A method of forming a semiconductor device, comprising:

proving a semiconductor substrate with a gate structure formed thereon;

blanket depositing at least one first dielectric layer overlying the semiconductor substrate without performing an etch process on the at least one first dielectric layer;

wherein, the at least one first dielectric layer comprises at least one first portion along at least one sidewall of the gate structure;

wherein, the at least one first dielectric layer comprises at least one second portion outside the gate structure along the surface of the semiconductor substrate; and

performing a first ion implantation process to form at least one first doped region in the semiconductor substrate laterally adjacent to the at least one first portion of the at least one first dielectric

layer, wherein the at least one second portion of the at least one first dielectric layer remains overlying the at least one first doped region.

11. The method of forming a semiconductor device of claim 10, further comprising performing an annealing process to activate ions of the at least one first doped region, wherein the at least one first dielectric layer becomes a densified material with an etch rate less than about 200 Angstroms/minute in a 100:1 HF solution.

12. The method of forming a semiconductor device of claim 10, wherein a thickness of the at least one first dielectric layer ranges from about 10 Angstroms to about 350 Angstroms.

13. The method of forming a semiconductor device of claim 10, wherein the at least one first dielectric layer is silicon oxide, silicon oxynitride, alternating layers of silicon oxide and silicon nitride, or combinations thereof.

14. The method of forming a semiconductor device of claim 10, further comprising:

depositing at least one second dielectric layer overlying the at least one first dielectric layer;

etching the at least one second dielectric layer to form at least one sidewall spacer along the at least one sidewall of the gate structure; and

performing a second ion implantation process to form at least one second doped region in the semiconductor substrate laterally adjacent to the at least one sidewall spacer.

15. The method of forming a semiconductor device of claim 10, wherein the at least one second dielectric layer is silicon oxide, silicon oxynitride, alternating layers of silicon oxide and silicon nitride, or combinations thereof.

16. An integrated circuit transistor, comprising:

a semiconductor substrate having a gate structure;

at least one dielectric layer overlying the semiconductor substrate, wherein the at least one dielectric layer comprises at least one first portion along at least one sidewall of the gate structure;

at least one first doped region in the semiconductor substrate laterally adjacent to the at least one first portion of the at least one dielectric layer;

a sidewall spacer overlying the at least one dielectric layer along the at least one sidewall of the gate structure; and

at least one second doped region formed in the semiconductor substrate laterally adjacent to the sidewall spacer;

wherein, the at least one dielectric layer is a densified material with an etch rate less than about 200 Angstroms/minute in a 100:1 HF solution.

17. The integrated circuit transistor of claim 16, wherein the at least one dielectric layer comprises at least one second portion which covers the at least one first doped region.

18. The integrated circuit transistor of claim 16, wherein the at least one dielectric layer is an L-shaped spacer extending from the at least one sidewall of the gate structure to the at least one first doped region.

19. The integrated circuit transistor of claim 16, wherein a thickness of the at least one dielectric layer ranges from about 10 Angstroms to about 350 Angstroms.

20. The integrated circuit transistor of claim 16, wherein the at least one dielectric layer is silicon oxide, silicon oxynitride, alternating layers of silicon oxide and silicon nitride, or combinations thereof.

21. The integrated circuit transistor of claim 16, wherein the at least one dielectric layer is a TEOS oxide layer.

22. The integrated circuit transistor of claim 16, wherein the sidewall spacer is silicon oxide, silicon

oxynitride, alternating layers of silicon oxide and silicon nitride, or combinations thereof.